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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,442	04/15/2004	Takayuki Iwasaki	501.38166CX1	6287

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EXAMINER

RICHARDS, N DREW

ART UNIT	PAPER NUMBER
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2815

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/824,442

Applicant(s)

IWASAKI ET AL.

Examiner

N. Drew Richards

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) 4,5,7-11 and 13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,6 and 12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 April 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to the previous rejection(s) of claim(s) 1-3, 6 and 12 under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bhatnagar et al. (US Patent No. 5,780,878).

Drawings

2. Figures 2-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "the blocking state" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. Since the claim has not defined the metes and bounds of "the blocking state" this limitation renders the claim indefinite.

Claim 12 lines 18-20 recite the second semiconductor region being in contact with itself. It is unclear how this limitation is intended to limit the scope of the invention or further describe applicant's invention since every structure is necessarily in contact with itself.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 6 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhatnagar et al. (US Patent No. 5,780,878).

With regard to claim 1, Bhatnagar et al. disclose in figure 1, for example, a static induction transistor comprising:

- a semiconductor substrate with an energy band gap greater than that of silicon (silicon carbide, see column 2 lines 50-52)
- a first semiconductor region 15 of a first conduction type (N-)
- a second semiconductor region 26 of a first conduction type, positioned on the surface of the first semiconductor region and having an impurity concentration higher than that of the first semiconductor region (N+, see column 3 line 18)
- a first gate region (30 and 35 are considered the gate "region") of a second conduction type positioned on the surface of the first semiconductor region
- a second gate region 16 of a second conduction type, including a projection of the second semiconductor region and partially including a projection of the first gate region within the first semiconductor region
- a drain electrode 13 connected electrically to the first semiconductor region
- a source electrode 28 connected electrically to the second semiconductor region
- a gate electrode (gate) connected electrically to the first gate region

- characterized in that the second semiconductor region and the first gate region are in contact with each other on the surface of the first semiconductor region.

With regard to claim 2, at a "blocking state" the potential of the second gate region is in a floating state, or at the same potential as that of the second semiconductor region or the first gate region.

With regard to claim 3, the length of a part, in the second gate region, overlapping the projection of the second semiconductor region is larger than the width of a part of the first semiconductor region disposed between the first gate region and the second gate region.

With regard to claim 6, a semiconductor material of the substrate is silicon carbide, diamond or gallium nitride.

With regard to claim 12, Bhatnagar et al. disclose in figure 1, for example, a static induction transistor comprising:

- a semiconductor substrate with an energy band gap greater than that of silicon (silicon carbide, see column 2 lines 50-52)
- a first semiconductor region 15 of a first conduction type (N-)
- a second semiconductor region 26 of a first conduction type, positioned on the surface of the first semiconductor region and having an impurity

concentration higher than that of the first semiconductor region (N⁺, see column 3 line 18)

- a first gate region (30 and 35 are considered the gate "region") of a second conduction type positioned on the surface of the first semiconductor region
- a second gate region 16 of a second conduction type, including a projection of the second semiconductor region and partially including a projection of the first gate region within the first semiconductor region
- a drain electrode 13 connected electrically to the first semiconductor region
- a source electrode 28 connected electrically to the second semiconductor region
- a gate electrode (gate) connected electrically to the first gate region
- characterized in that the second semiconductor region and the second semiconductor region are in contact with each other on the surface of the first semiconductor region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


N. DREW RICHARDS
PRIMARY EXAMINER